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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,026	03/31/2004	Jianping Xu	42P17342	9324

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EXAMINER	
HAGAN, SEAN P	

ART UNIT	PAPER NUMBER
2828	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,026	XU ET AL.	
	Examiner	Art Unit	
	SEAN HAGAN	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *14-17,19,20 and 25-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,18,21-24,32 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 through 33 originally filed 31 March 2004. Claims 1 through 13, 18, 21 through 24, 32, and 33 elected for examination in response received 19 March 2009. Claims 1 through 33 are pending in this application. Claims 1, 9, 18, and 23 amended by amendment received 1 February 2010. Claims 1 through 13, 18, 21 through 24, 32, and 33 are addressed in this action.

Response to Arguments

2. Applicant's arguments have been fully considered; they are persuasive.

3. Applicants argue that the subject matter included by amendment is not taught by the prior art previously cited. Examiner concedes this point, but notes further art which supports the conclusion that these features would have been obvious to one of ordinary skill in the art at the time of invention. A rejection of the presently addressed claims over relevant art is presented below.

4. As such, all claims are addressed as follows:

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1, 2, 3, 4, 5, 6, 7, 8, 23, 32, and 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US Pub. 2001/0021051) in view of Comerford (US Patent 4,592,057) and further in view of Chun et al. (Chun, US Patent 6,294,933).

7. ***Regarding claim 1,*** Kim discloses, "Serializing an N-bit data to generate a digital voltage sequence" (p. [0019]). "Converting the digital voltage sequence to a first current signal having an adjustable bias mode and a separately adjustable modulation mode" (p. [0054], lines 5-8). "Driving a first laser using said first current signal to generate a first optical signal transmission" (p. [0019]). "Converting a second optical signal reception into a first single-ended voltage signal" (p. [0053]). Kim does not disclose, "Wherein said modulation mode is controlled by a modulation control circuit." "Said bias mode is controlled by a separate bias control circuit." Comerford discloses, "Wherein said modulation mode is controlled by a modulation control circuit" (col. 8, lines 14-45). "Said bias mode is controlled by a separate bias control circuit" (col. 8, lines 14-45). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Kim with the teachings of Comerford. The specific splitting of bias and modulation current as taught by Comerford would enhance the teachings of Kim by allowing the laser diode to be regulated above threshold while maintaining modulation depth.

8. The combination of Kim and Comerford does not disclose, "Complimentary coupling said first single-ended voltage signal with a second single-ended voltage signal to generated a differential data voltage signal." "Resistively coupling said first and

second single-ended voltage signals to attenuate a common signal noise." Chun discloses, "Complimentary coupling said first single-ended voltage signal with a second single-ended voltage signal to generated a differential data voltage signal" (col. 3, lines 28-38). "Resistively coupling said first and second single-ended voltage signals to attenuate a common signal noise" (col. 6, lines 20-24). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of the combination of Kim and Comerford with the teachings of Chun. Clock recovery as detailed in Chun would enhance the teachings of Kim by reducing the effect of noise. (Chun, col. 6, lines 20-24)

9. ***Regarding claim 2,*** Kim discloses, "Generating a digital clock signal" (p. [0049]). "Using the digital clock signal to generate the digital voltage sequence from the N-bit data" (Fig. 11, pt. 176). "Converting the digital clock signal to a second current signal having an adjustable bias mode and an adjustable modulation mode" (p. [0054], lines 5-8). "Driving a second laser using said second current signal to generate a third optical signal transmission" (Fig. 11, pt. 180e).

10. ***Regarding claim 3,*** Kim discloses, "Adjusting said modulation mode of the second current signal" (p. [0054]).

11. ***Regarding claim 4,*** Kim discloses, "Adjusting said bias mode of the second current signal" (p. [0054]).

12. ***Regarding claim 5,*** Kim discloses, "Converting the third optical signal reception into a third single-ended voltage signal" (p. [0058]).

13. The combination of Kim and Comerford does not disclose, "Complimentary coupling said third single-ended voltage signal with a fourth single-ended voltage signal to generate a differential clock signal." "Recovering the digital clock signal from the differential clock signal." Chun discloses, "Complimentary coupling said third single-ended voltage signal with a fourth single-ended voltage signal to generate a differential clock signal" (col. 3, lines 28-38). "Recovering the digital clock signal from the differential clock signal" (col. 3, lines 17-21). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of the combination of Kim and Comerford with the teachings of Chun for the reasons provided above regarding claim 1.

14. ***Regarding claim 6,*** Kim discloses, "Generating a plurality of clock phases from the differential clock signal in a delay locked loop" (p. [0073]). "Interpolating the plurality of clock phases to align a clock edge of the digital clock signal with respect to the differential data voltage signal" (p. [0067]).

15. ***Regarding claim 7,*** Kim discloses, "Adjusting said modulation mode of the first current signal by setting one or more modulation control inputs" (p. [0054]).

16. ***Regarding claim 8,*** Kim discloses, "Adjusting said bias mode of the first current signal by setting one or more bias control inputs" (p. [0054]).

17. ***Regarding claim 23,*** Kim discloses, "Said laser driver to receive a first digital voltage sequence and to generate a first current signal having a bias mode adjustable by a bias control circuit" (p. [0019]). "A laser to generate a first optical signal responsive to the first current signal of the laser driver" (p. [0019]). "A first photo-detector to receive a second optical signal and to generate a second current signal" (p. [0058]). "A clock recovery circuit having a phase interpolator to generate an aligned clock signal for said first differential voltage signal" (p. [0067]). "A sampler circuit to generate a second digital voltage sequence responsive at least in part to the aligned clock signal and the first differential voltage signal" (p. [0073]). Kim does not disclose, "A laser driver having a bias control and a modulation control separate from said bias control." "A modulation mode adjustable by a modulation control circuit separate from said bias control circuit." Comerford discloses, "A laser driver having a bias control and a modulation control separate from said bias control" (col. 8, lines 14-45). "A modulation mode adjustable by a modulation control circuit separate from said bias control circuit" (col. 8, lines 14-45). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Kim with the teachings of Comerford for the reasons provided above regarding claim 1.

18. The combination of Kim and Comerford does not disclose, "A first transimpedance amplifier circuit to convert the second current signal to a first differential

voltage signal." Chun discloses, "A first transimpedance amplifier circuit to convert the second current signal to a first differential voltage signal" (col. 3, lines 28-38). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of the combination of Kim and Comerford with the teachings of Chun for the reasons provided above regarding claim 1.

19. ***Regarding claim 32,*** the combination of Kim, Comerford, and Chun does not disclose, "A second photo-detector to receive a third optical signal and to generate a third current signal." "A second transimpedance amplifier circuit to convert the third current signal to a differential clock signal." "Said clock recovery circuit having said phase interpolator to generate the aligned clock signal for said first differential voltage signal from the differential clock signal." It would have been obvious to one of ordinary skill in the art to duplicate the clock transmission means detailed in Kim so as to accomplish the clock processing means detailed by Chun, since it has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

20. ***Regarding claim 33,*** Kim discloses, "A delay locked loop to generate a plurality of clock phases from the differential clock signal" (p. [0073]). "Said phase interpolator to generate the aligned clock signal from the plurality of clock phases" (p. [0067]).

21. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Comerford.

22. ***Regarding claim 9,*** Kim discloses, "A phase locked loop circuit to generate a clock signal" (p. [0049]). "A serializer circuit to receive the clock signal and to convert an N-bit data to a digital voltage sequence" (p. [0019]). "Said laser driver to receive the digital voltage sequence and to generate a current signal having a bias mode adjustable by a bias control circuit" (p. [0019]). "A laser to generate an optical signal responsive to the current signal of the laser driver" (Fig. 2, pt. 180). Kim does not disclose, "A laser driver having a bias control and a modulation control distinct from said bias control." "A modulation mode separately adjustable by a modulation control circuit that is distinct from said bias control circuit." Comerford discloses, "A laser driver having a bias control and a modulation control distinct from said bias control" (col. 8, lines 14-45). "A modulation mode separately adjustable by a modulation control circuit that is distinct from said bias control circuit" (col. 8, lines 14-45). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Kim with the teachings of Comerford for the reasons provided above regarding claim 1.

23. Claims 10 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Comerford and further in view of Bosch et al. (Bosch, US Patent 6,130,562).

24. ***Regarding claim 10,*** the combination of Kim and Comerford does not disclose, "A buffered level shifter circuit tunable through k+1 control signals to shift an input of the laser driver to a controlled voltage level at a controlled rate and with adjustable impedance responsive to a transition of said digital voltage sequence." Bosch discloses, "A buffered level shifter circuit tunable through k+1 control signals to shift an input of the laser driver to a controlled voltage level at a controlled rate and with adjustable impedance responsive to a transition of said digital voltage sequence" (Fig. 2). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of the combination of Kim and Comerford with the teachings of Bosch. A level shifter as provided by Bosch would enhance the teachings of Kim by providing a means to digitally control the level of modulation.

25. ***Regarding claim 13,*** the combination of Kim, Comerford, and Bosch does not disclose, "A plurality of capacitors coupled with the bias control to reduce a frequency dependent component of impedance." It would have been obvious to one of ordinary skill in the art to provide a capacitor bank to provide a low resistance means to achieve high capacitance, since it was known in the art that parallel capacitors have a total capacitance equal to the sum of the constituent components while the reciprocal of total resistance equals the sum of the reciprocals of the constituent components.

26. Claims 11 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Comerford in view of Bosch and further in view of Tsai (US Patent 6,735,228).

27. ***Regarding claim 11,*** the combination of Kim, Comerford, and Bosch does not disclose, "A CMOS modulation circuit having a pMOSFET, a first nMOSFET and a second nMOSFET." "The CMOS modulation circuit to cause the current signal of the modulation mode to flow from a laser power source through the first nMOSFET and second nMOSFET responsive to the input of the laser driver being shifted to a first voltage level." "To causes the current signal of the bias mode to flow from the laser power source through the bias control when another current flows from a second power source through the pMOSFET responsive to the input of the laser driver being shifted to a second voltage level." Tsai discloses, "A CMOS modulation circuit having a pMOSFET, a first nMOSFET and a second nMOSFET" (Fig. 4, pts. 430, 420, and Q507). "The CMOS modulation circuit to cause the current signal of the modulation mode to flow from a laser power source through the first nMOSFET and second nMOSFET responsive to the input of the laser driver being shifted to a first voltage level" (Fig. 3a). "To causes the current signal of the bias mode to flow from the laser power source through the bias control when another current flows from a second power source through the pMOSFET responsive to the input of the laser driver being shifted to a second voltage level" (Fig. 3a). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of the combination of Kim,

Comerford, and Bosch with the teachings of Tsai. The driving circuit of Tsai would have been suitable for use with the teachings of Kim and Bosch. The selection of something based on its known suitability for its intended use has been held to support a prima facie case of obviousness. *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

28. ***Regarding claim 12,*** the combination of Kim, Comerford, and Bosch does not disclose, "An input gate of the third nMOSFET is coupled with the second power source to reduce an overshoot of the current signal." Tsai discloses, "An input gate of the third nMOSFET is coupled with the second power source to reduce an overshoot of the current signal" (Fig. 4, pt. Q508). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of the combination of Kim, Comerford, and Bosch with the teachings of Tsai for the reasons provided above regarding claim 11.

29. Claims 18, 21, and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Bartur et al. (Bartur, US Pub. 2002/0027689).

30. ***Regarding claim 18,*** Kim discloses, "A first photo-detector to receive a first optical signal and to generate a first current signal" (p. [0058]). "A first transimpedance amplifier circuit to convert the first current signal to a first differential voltage signal" (p. [0058]). "A clock recovery circuit having a phase interpolator to generate an aligned

clock signal for said first differential voltage signal" (p. [0067]). "A deserializer circuit to receive the digital voltage sequence and to generate an N-bit data" (p. [0058]). Kim does not disclose, "Wherein the first transimpedance amplifier circuit is configured to produce a differential voltage and is further configured to difference the components of the differential voltage to produce said first differential voltage signal." "A sampler circuit to receive the aligned clock signal and to receive the differential voltage signal and to generate a digital voltage sequence." Bartur discloses, "Wherein the first transimpedance amplifier circuit is configured to produce a differential voltage and is further configured to difference the components of the differential voltage to produce said first differential voltage signal" (p. [0042]). "A sampler circuit to receive the aligned clock signal and to receive the differential voltage signal and to generate a digital voltage sequence" (p. [0042]). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Kim with the teachings of Bartur. Clock recovery as detailed in Bartur would enhance the teachings of Kim by reducing the effect of noise.

31. ***Regarding claim 21,*** the combination of Kim and Bartur does not disclose, "A second photo-detector to receive a second optical signal and to generate a second current signal." "A second transimpedance amplifier circuit to convert the second current signal to a differential clock signal." "Said clock recovery circuit having said phase interpolator to generate the aligned clock signal for said first differential voltage signal from the differential clock signal." It would have been obvious to one of ordinary

skill in the art to duplicate the clock transmission means detailed in Kim so as to accomplish the clock processing means detailed by Chun, since it has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

32. ***Regarding claim 22,*** Kim discloses, "A delay locked loop to generate a plurality of clock phases from the differential clock signal" (p. [0073]). "Said phase interpolator to generate the aligned clock signal from the plurality of clock phases" (p. [0067]).

33. Claim 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Comerford in view of Chun and further in view of Bosch.

34. ***Regarding claim 24,*** the combination of Kim, Comerford, and Chun does not disclose, "A tunable buffered level shifter to shift an input of the laser driver to a controlled voltage level responsive to a transition of said first digital voltage sequence." Bosch discloses, "A tunable buffered level shifter to shift an input of the laser driver to a controlled voltage level responsive to a transition of said first digital voltage sequence" (Fig. 2). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of the combination of Kim, Comerford, and Chun with the teachings of Bosch. A level shifter as provided by Bosch would enhance the teachings of Kim and Chun by providing a means to digitally control the level of modulation.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SEAN HAGAN whose telephone number is (571)270-1242. The examiner can normally be reached on Monday-Friday 7:30 - 5:00.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun O. Harvey can be reached on 571-272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. H./
Examiner, Art Unit 2828

/Minsun Harvey/
Supervisory Patent Examiner, Art Unit 2828